# Current Output/ Serial Input, 16-/14-Bit DAC

# AD5543/AD5553

## FEATURES

**16-bit resolution AD5543**
**14-bit resolution AD5553**
**±1 LSB DNL**
**±1 LSB INL**
**Low noise: 12 nV/√Hz**
**Low power: $I_{DD}$ = 10 µA**
**0.5 µs settling time**
**4Q multiplying reference input**
**2 mA full-scale current ± 20%, with $V_{REF}$ = 10 V**
**Built-in RFB facilitates voltage conversion**
**3-wire interface**
**Ultracompact MSOP-8 and SOIC-8 packages**

## APPLICATIONS

**Automatic test equipment**
**Instrumentation**
**Digitally controlled calibration**
**Industrial control PLCs**

## GENERAL DESCRIPTION

The AD5543/AD5553 are precision 16-/14-bit, low power, current output, small form factor digital-to-analog converters (DAC). They are designed to operate from a single 5 V supply with a ±10 V multiplying reference.

The applied external reference, $V_{REF}$, determines the full-scale output current. An internal feedback resistor ($R_{FB}$) facilitates the R-2R and temperature tracking for voltage conversion when combined with an external op amp.

A serial-data interface offers high speed, 3-wire microcontroller-compatible inputs using serial data in (SDI), clock (CLK), and chip select ($\overline{CS}$).

The AD5543/AD5553 are packaged in ultracompact (3 mm × 4.7 mm) MSOP-8 and SOIC-8 packages.

## FUNCTIONAL BLOCK DIAGRAM

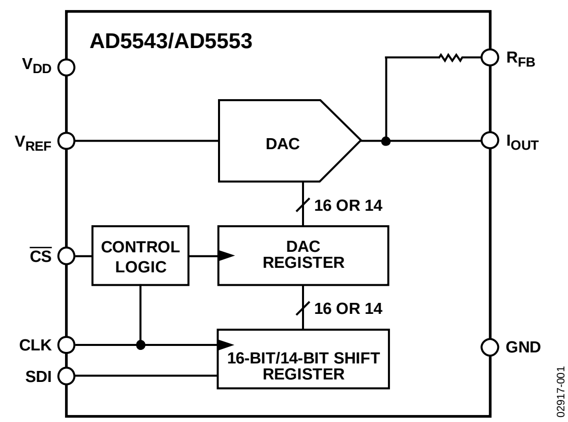


*Figure 1.*

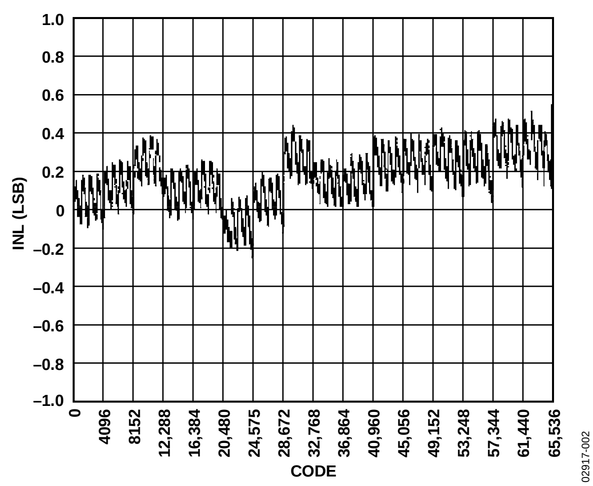


*Figure 2. Integral Nonlinearity*

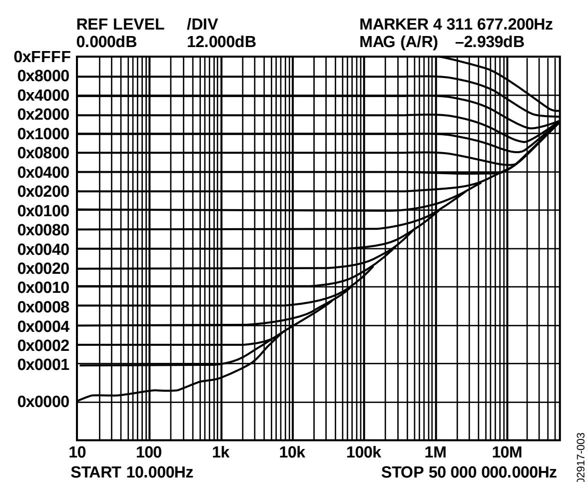


*Figure 3. Reference Multiplying Bandwidth*


**Rev. C**





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Updated Outline Dimensions ... 14
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**2/03—Rev. 0 to Rev. A**

Changes to Ordering Guide ... 3

**12/02—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 5 V ± 10%, $V_{SS}$ = 0 V, $I_{OUT}$ = virtual GND, GND = 0 V, $V_{REF}$ = 10 V, $T_A$ = full operating temperature range, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Condition | 5 V ± 10% | Unit |
|---|---|---|---|---|
| STATIC PERFORMANCE[1] | | | | |
| Resolution | N | 1 LSB = $V_{REF}/2^{16}$ = 153 µV when $V_{REF}$ = 10 V (AD5543) | 16 | Bits |
| | | 1 LSB = $V_{REF}/2^{14}$ = 610 µV when $V_{REF}$ = 10 V (AD5553) | 14 | Bits |
| Relative Accuracy | INL | Grade: AD5553C | ±1 | LSB max |
| | | Grade: AD5543C | ±1 | LSB max |
| | | Grade: AD5543B | ±2 | LSB max |
| Differential Nonlinearity | DNL | Monotonic | ±1 | LSB max |
| Output Leakage Current | $I_{OUT}$ | Data = 0x0000, $T_A$ = 25°C | 10 | nA max |
| | | Data = 0x0000, $T_A$ = $T_A$ max | 20 | nA max |
| Full-Scale Gain Error | $G_{FSE}$ | Data = 0xFFFF | ±1/±4 | mV typ/max |
| Full-Scale Tempco[2] | $TCV_{FS}$ | | 1 | ppm/°C typ |
| REFERENCE INPUT | | | | |
| $V_{REF}$ Range | $V_{REF}$ | | −15/+15 | V min/max |
| Input Resistance | $R_{REF}$ | | 5 | kΩ typ[3] |
| Input Capacitance[2] | $C_{REF}$ | | 5 | pF typ |
| ANALOG OUTPUT | | | | |
| Output Current | $I_{OUT}$ | Data = 0xFFFF for AD5543 | 2 | mA typ |
| | | Data = 0x3FFF for AD5553 | | |
| Output Capacitance[2] | $C_{OUT}$ | Code dependent | 200 | pF typ |
| LOGIC INPUTS AND OUTPUT | | | | |
| Logic Input Low Voltage | $V_{IL}$ | | 0.8 | V max |
| Logic Input High Voltage | $V_{IH}$ | | 2.4 | V min |
| Input Leakage Current | $I_{IL}$ | | 10 | µA max |
| Input Capacitance[2] | $C_{IL}$ | | 10 | pF max |
| INTERFACE TIMING[2, 4] | | | | |
| Clock Input Frequency | $f_{CLK}$ | | 50 | MHz |
| Clock Width High | $t_{CH}$ | | 10 | ns min |
| Clock Width Low | $t_{CL}$ | | 10 | ns min |
| $\overline{CS}$ to Clock Setup | $t_{CSS}$ | | 0 | ns min |
| Clock to $\overline{CS}$ Hold | $t_{CSH}$ | | 10 | ns min |
| Data Setup | $t_{DS}$ | | 5 | ns min |
| Data Hold | $t_{DH}$ | | 10 | ns min |
| SUPPLY CHARACTERISTICS | | | | |
| Power Supply Range | $V_{DD\ RANGE}$ | | 4.5/5.5 | V min/max |
| Positive Supply Current | $I_{DD}$ | Logic inputs = 0 V | 10 | µA max |
| Power Dissipation | $P_{DISS}$ | Logic inputs = 0 V | 0.055 | mW max |
| Power Supply Sensitivity | $P_{SS}$ | $\Delta V_{DD}$ = ±5% | 0.006 | %/% max |

| Parameter | Symbol | Condition | 5 V ± 10% | Unit |
|---|---|---|---|---|
| AC CHARACTERISTICS[4] | | | | |
| Output Voltage Settling Time | $t_S$ | To ±0.1% of full scale, | 0.5 | µs typ |
| | | Data = 0x0000 to 0xFFFF to 0x0000 for AD5543 | | |
| | | Data = 0x0000 to 0x3FFF to 0x0000 for AD5553 | | |
| Reference Multiplying BW | BW | $V_{REF}$ = 5 V p-p, data = 0xFFFF | 4 | MHz typ |
| DAC Glitch Impulse | Q | $V_{REF}$ = 0 V, data = 0x7FFF to 0x8000 for AD5543 | 7 | nV-sec |
| Feedthrough Error | $V_{OUT}/V_{REF}$ | Data = 0x0000, $V_{REF}$ = 100 mV rms, same channel | −65 | dB |
| Digital Feedthrough | Q | $C_S$ = 1, and $f_{CLK}$ = 1 MHz | 7 | nV-sec |
| Total Harmonic Distortion | THD | $V_{REF}$ = 5 V p-p, data = 0xFFFF, f = 1 kHz | −85 | dB typ |
| Output Spot Noise Voltage | $e_N$ | f = 1 kHz, BW = 1 Hz | 12 | nV/√Hz |

[1] All static performance tests (except $I_{OUT}$) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5543 $R_{FB}$ terminal is tied to the amplifier output. The +IN op amp is grounded, and the DAC $I_{OUT}$ is tied to the −IN op amp. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and are not subject to production testing.
[3] All ac characteristic tests are performed in a closed-loop system using an AD841 I-to-V converter amplifier.
[4] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

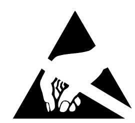
# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +8 V |
| $V_{REF}$ to GND | −18 V to +18 V |
| Logic Inputs to GND | −0.3 V to +8 V |
| $V(I_{OUT})$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supplies | ±50 mA |
| Package Power Dissipation | $(T_{J\,Max} - T_A)/\theta_{JA}$ |
| Thermal Resistance, $\theta_{JA}$ | |
| 8-Lead Surface Mount (MSOP-8) | 150°C/W |
| 8-Lead Surface Mount (SOIC-8) | 100°C/W |
| Maximum Junction Temperature ($T_{J\,Max}$) | 150°C |
| Operating Temperature Range | |
| Model B and Model C | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature | |
| RN-8, RM-8 (Vapor Phase, 60 sec) | 215°C |
| RN-8, RM-8 (Infrared, 15 sec) | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

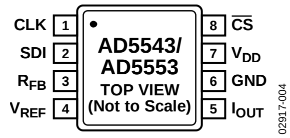



*Figure 4. Pin Configuration*

**Table 3. Pin Function Descriptions**

| Pin No. | Mnemonic | Function |
|---|---|---|
| 1 | CLK | Clock Input. Positive-edge triggered, clocks data into shift register. |
| 2 | SDI | Serial Register Input. Data loads directly into the shift register MSB first. Extra leading bits are ignored. |
| 3 | $R_{FB}$ | Internal Matching Feedback Resistor. Connects to an external op amp for voltage output. |
| 4 | $V_{REF}$ | DAC Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code. |
| 5 | $I_{OUT}$ | DAC Current Output. Connects to inverting terminal of external precision I-to-V op amp for voltage output. |
| 6 | GND | Analog and Digital Ground. |
| 7 | $V_{DD}$ | Positive Power Supply Input. Specified range of operation at 5 V ± 10%. |
| 8 | $\overline{CS}$ | Chip Select. Active low digital input. Transfers shift-register data to DAC register on rising edge. See Table 4 for operation. |

## TYPICAL PERFORMANCE CHARACTERISTICS

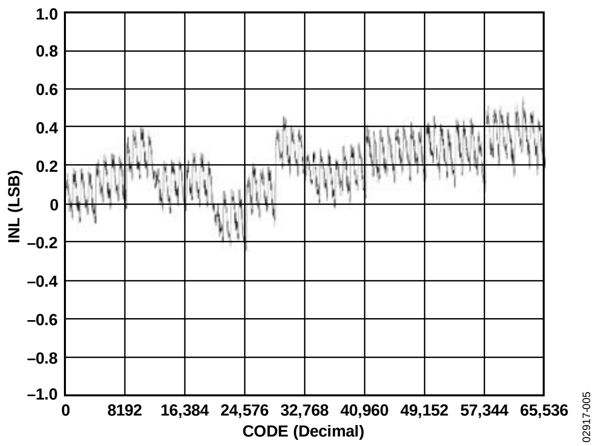



*Figure 5. AD5543 Integral Nonlinearity Error*

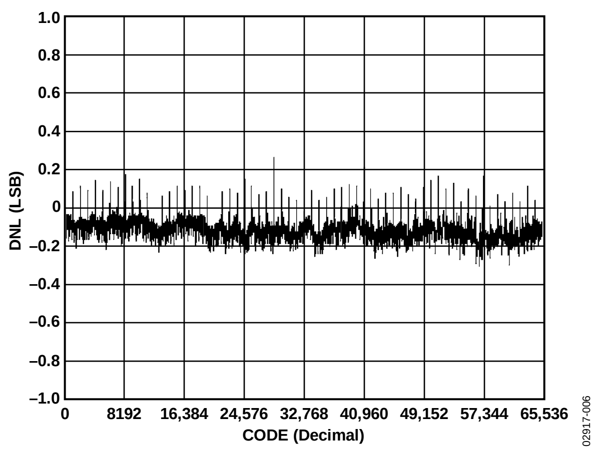



*Figure 6. AD5543 Differential Nonlinearity Error*

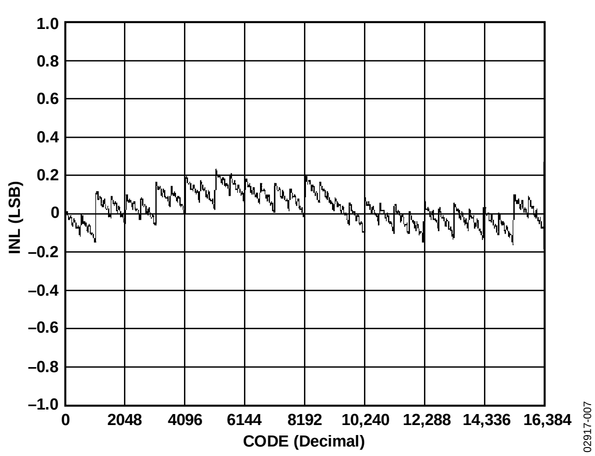



*Figure 7. AD5553 Integral Nonlinearity Error*

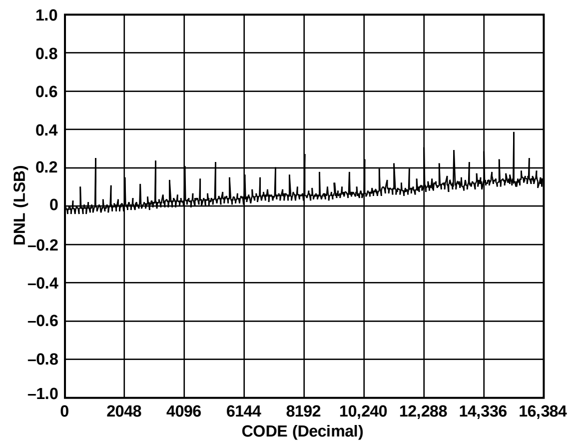



*Figure 8. AD5553 Differential Nonlinearity Error*

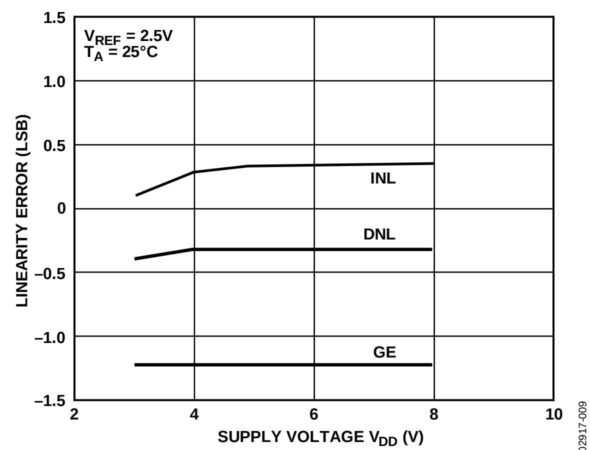



*Figure 9. Linearity Error vs. $V_{DD}$*

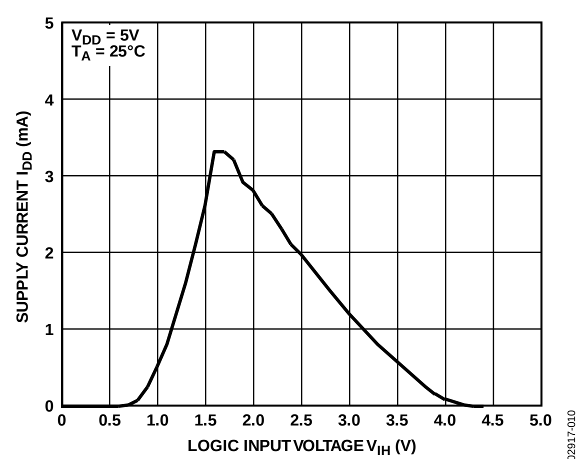



*Figure 10. Supply Current vs. Logic Input Voltage*

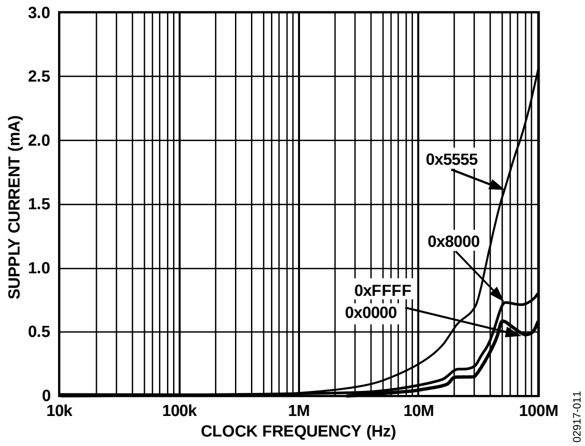



Figure 11. AD5543 Supply Current vs. Clock Frequency

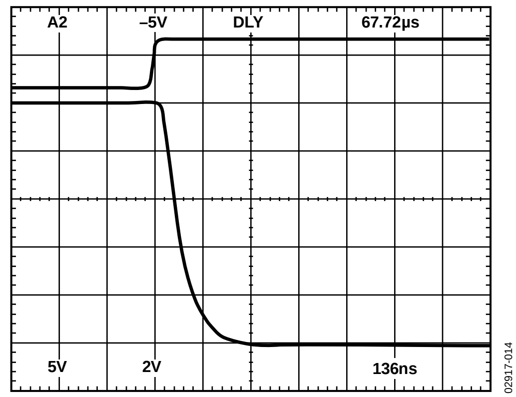



Figure 14. Settling Time

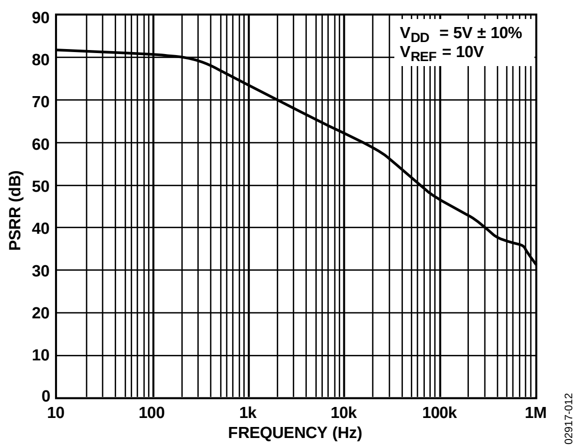



Figure 12. Power Supply Rejection Ratio vs. Frequency

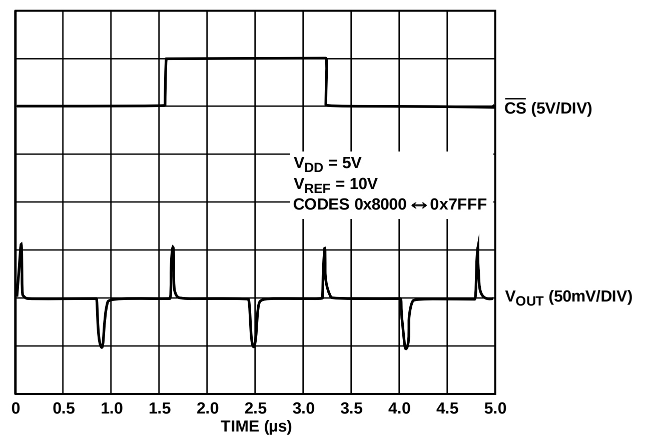



Figure 15. Midscale Transition and Digital Feedthrough

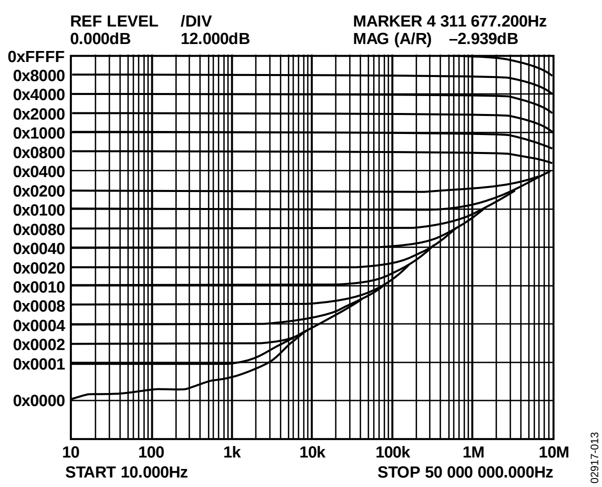



Figure 13. Reference Multiplying Bandwidth

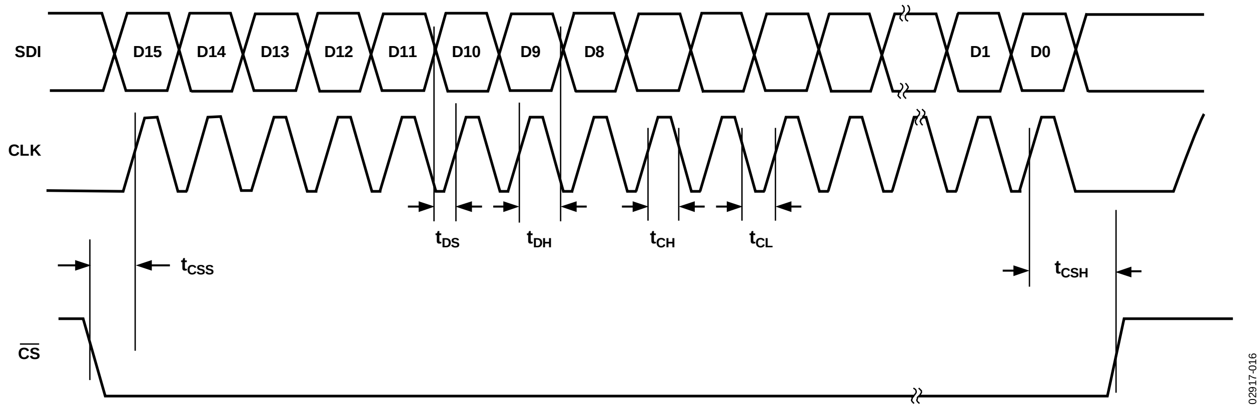



*Figure 16. AD5543 Timing Diagram*

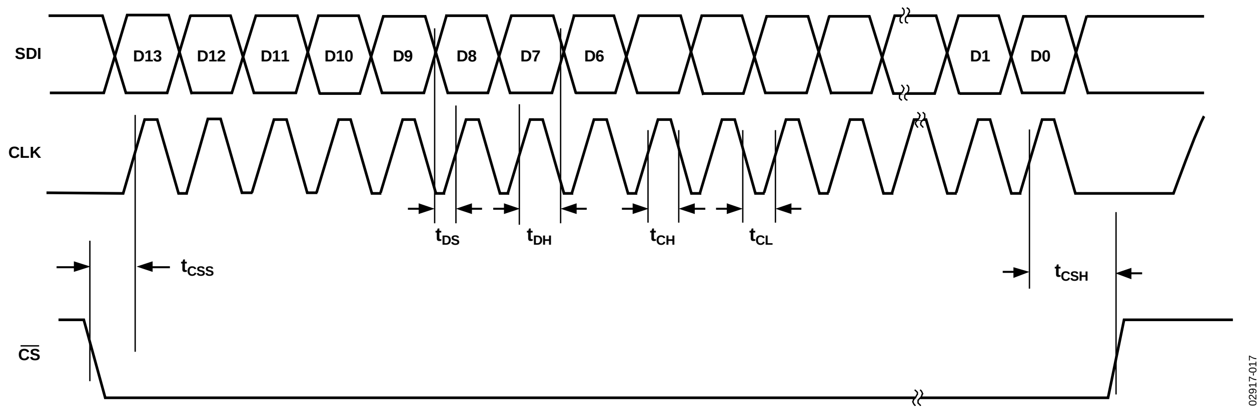



*Figure 17. AD5553 Timing Diagram*

**Table 4. Control-Logic Truth Table**

| CLK | $\overline{CS}$ | Serial Shift Register Function | DAC Register |
|---|---|---|---|
| X | H | No effect | Latched |
| ↑+[1] | L | Shift register data advanced one bit | Latched |
| X[1] | H | No effect | Latched |
| X[1] | ↑+[1] | Shift register data transferred to DAC register | New data loaded from serial register |

[1] ↑+ = positive logic transition; X = don't care.

**Table 5. AD5543 Serial Input Register Data Format; Data is Loaded in the MSB-First Format**

| MSB | | | | | | | | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 6. AD5553 Serial Input Register Data Format; Data is Loaded in the MSB-First Format**

| MSB[1] | | | | | | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

[1] A full 16-bit data-word can be loaded into the AD5553 serial input register, but only the last 14 bits entered are transferred to the DAC register when $\overline{CS}$ returns to logic high.

# CIRCUIT OPERATION

The AD5543/AD5553 contain 16-/14-bit, current output, digital-to-analog converters (DAC), serial input registers, and DAC registers. Both converters use a 3-wire serial data interface.

## DAC SECTION

The DAC architecture uses a current steering R-2R ladder design. Figure 18 shows the typical equivalent DAC structure. The DAC contains a matching feedback resistor for use with an external op amp (see Figure 19). With $R_{FB}$ and $I_{OUT}$ terminals connected to the op amp output and inverting node, respectively, a precision voltage output is achieved as

$$V_{OUT} = -V_{REF} \times D/65{,}536 \ (AD5543) \quad (1)$$

$$V_{OUT} = -V_{REF} \times D/16{,}384 \ (AD5553) \quad (2)$$

Note that the output voltage polarity is the opposite of the $V_{REF}$ polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The $V_{DD}$ power pin is only used by the internal logic to drive the on and off states of the DAC switches.

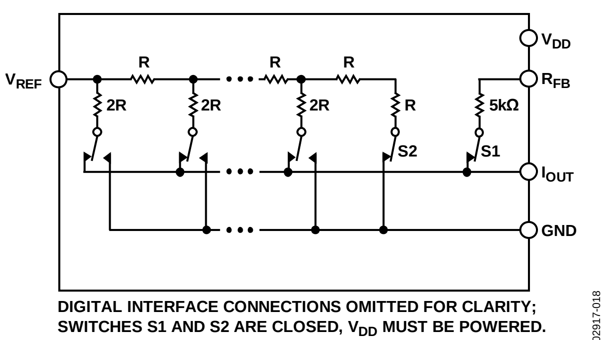



Figure 18. Equivalent R-2R DAC Circuit

Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users attempt to measure $R_{FB}$, power must be applied to $V_{DD}$ to achieve continuity.

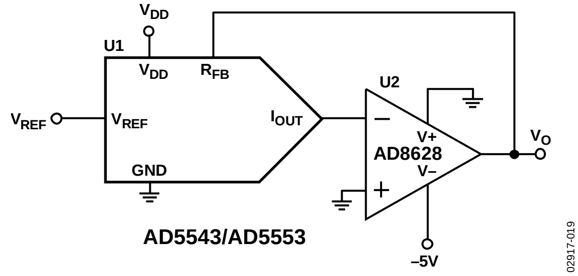



Figure 19. Voltage Output Configuration

These DACs are also designed to accommodate ac reference input signals. The AD5543 accommodates input reference voltages in the range of −12 V to +12 V. The reference voltage inputs exhibit a constant nominal input resistance value of 5 kΩ ± 30%. The DAC output ($I_{OUT}$) is code-dependent, producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the AD5543 on the inverting input node of the amplifier. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. To maintain good analog performance, power supply bypassing of 0.01 μF to 0.1 μF ceramic or chip capacitors, in parallel with a 1 μF tantalum capacitor, is recommended. Due to degradation of power supply rejection ratio (PSRR) in frequency, users must avoid using switching power supplies.

# SERIAL DATA INTERFACE

The AD5543/AD5553 use a 3-wire ($\overline{CS}$, SDI, CLK) serial data interface. New serial data is clocked into the serial input register in a 16-bit data-word format for the AD5543. The MSB is loaded first. Table 5 defines the 16 data-word bits. Data is placed on the SDI pin and clocked into the register on the positive clock edge of CLK, subject to the data setup-and-hold time requirements that are specified in the interface timing specifications. Only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin is strobed to transfer the serial register data to the DAC register. Because most microcontrollers output serial data in 8-bit bytes, two data bytes can be written to the AD5543/ AD5553. After loading the serial register, the rising edge of $\overline{CS}$ transfers the serial register data to the DAC register; during this strobe, the CLK should not be toggled. For the AD5553, with 16-bit clock cycles, the two LSBs are ignored.

## ESD PROTECTION CIRCUITS

All logic input pins contain back-biased ESD protection Zener diodes that are connected to ground (GND) and $V_{DD}$ as shown in Figure 20.

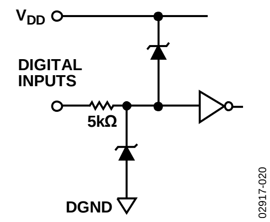



*Figure 20. Equivalent ESD Protection Circuits*

## PCB LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length PCB layout design. The leads to the input should be as short as possible to minimize IR drop and stray inductance.

It is also essential to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 μF to 0.1 μF disc or chip ceramic capacitors. Low-ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

The PCB metal traces between $V_{REF}$ and $R_{FB}$ should also be matched to minimize gain error.

# APPLICATIONS INFORMATION

## STABILITY

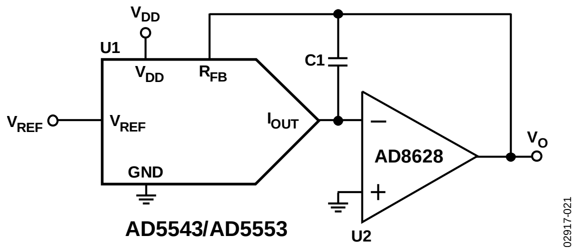



*Figure 21. Optional Compensation Capacitor for Gain Peaking Prevention*

In the I-to-V configuration, the $I_{OUT}$ of the DAC and the inverting node of the op amp must be connected as close as possible to each other, and proper PCB layout technique must be employed. Since every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP and, there is excessive parasitic capacitance at the inverting node.

An optional compensation capacitor, C1, can be added for stability as shown in Figure 21. C1 should be found empirically, but 20 pF is generally adequate for the compensation.

## POSITIVE VOLTAGE OUTPUT

To achieve the positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the tolerance errors of the resistors. To generate a negative reference, the reference can be level-shifted by an op amp such that the $V_{OUT}$ and GND pins of the reference become the virtual ground and −2.5 V, respectively (see Figure 22).

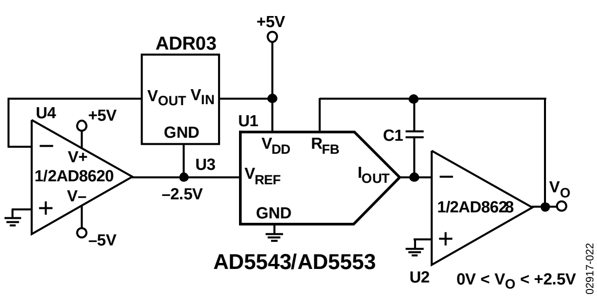



*Figure 22. Positive Voltage Output Configuration*

## BIPOLAR OUTPUT

The AD5543/AD5553 are inherently two-quadrant multiplying D/A converters. That is, they can easily be set up for unipolar output operation. The full-scale output polarity is the inverse of the reference input voltage.

In some applications, it may be necessary to generate the full four-quadrant multiplying capability or a bipolar output swing. This is easily accomplished by using an additional U4 external amplifier configured as a summing amplifier (see Figure 23). In this circuit, the second U4 amplifier provides a gain of 2 that increases the output span magnitude to 5 V. Biasing the external amplifier with a 2.5 V offset from the reference voltage results in a full four-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero ($V_{OUT}$ = −2.5 V) to midscale ($V_{OUT}$ = 0 V) to full-scale ($V_{OUT}$ = +2.5 V).

$$V_{OUT} = (D/32{,}768 - 1) \times V_{REF} \ (AD5543) \quad (3)$$

$$V_{OUT} = (D/16{,}384 - 1) \times V_{REF} \ (AD5553) \quad (4)$$

For the AD5543, the resistance tolerance becomes the dominant error of which users should be aware.

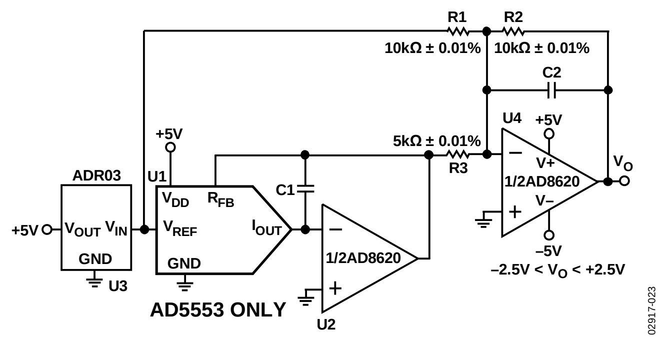



*Figure 23. Four-Quadrant Multiplying Application Circuit*

## PROGRAMMABLE CURRENT SOURCE

Figure 24 shows a versatile V-I conversion circuit using an improved Howland Current Pump. In addition to the precision current conversion it provides, this circuit enables a bidirectional current flow and high voltage compliance. This circuit can be used in 4 mA to 20 mA current transmitters with up to 500 Ω of load. In Figure 24, it can be shown that if the resistor network is matched, the load current is

$$I_L = \frac{(R2 + R3)/R1}{R3} \times V_{REF} \times D \quad (5)$$

R3 in theory can be made small to achieve the current needed within the U3 output current driving capability. This circuit is versatile such that AD8510 can deliver ±20 mA in both directions and the voltage compliance approaches 15 V, which is limited mainly by the supply voltages of U3. However, users must pay attention to the compensation. Without C1, it can be shown that the output impedance becomes

$$Z_O = \frac{R1' R3 (R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (6)$$

If the resistors are perfectly matched, $Z_O$ is infinite, which is desirable, and behaves as an ideal current source. On the other hand, if they are not matched, $Z_O$ can be either positive or negative. Negative can cause oscillation. As a result, C1 is needed to prevent the oscillation. For critical applications, C1 could be found empirically but typically falls in the range of a few picofarads (pF).

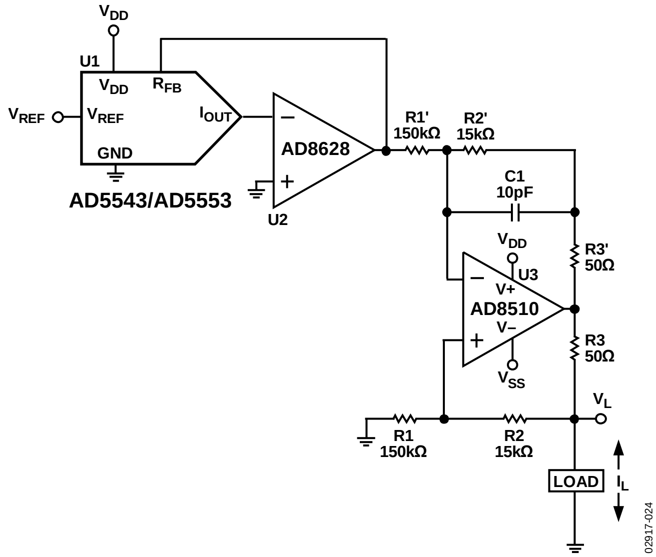



*Figure 24. Programmable Current Source with Bidirectional Current Control and High Voltage Compliance Capabilities*

# OUTLINE DIMENSIONS

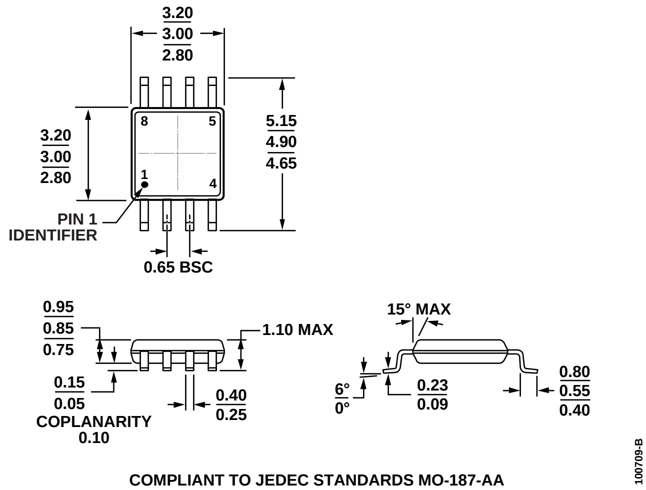



*Figure 25. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

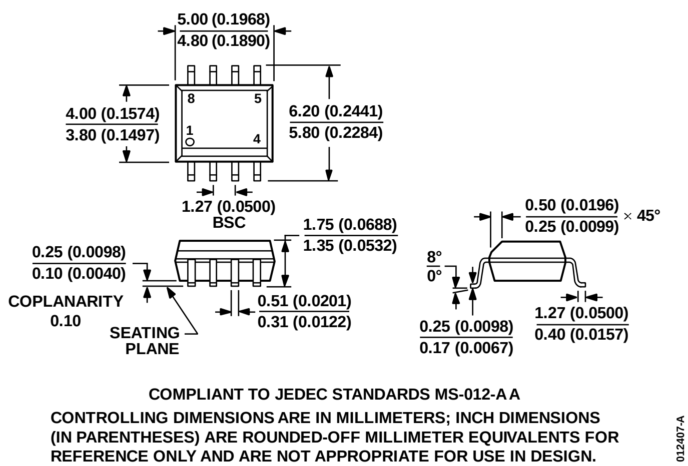



*Figure 26. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | INL (LSB) | RES (LSB) | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| AD5543CRMZ[2] | ±1 | 16 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DEV |
| AD5543CRMZ-REEL7[2] | ±1 | 16 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DEV |
| AD5543BR | ±2 | 16 | −40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD5543BRZ[2] | ±2 | 16 | −40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD5543BRM | ±2 | 16 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DXB |
| AD5543BRM-REEL7 | ±2 | 16 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DXB |
| AD5543BRMZ[2] | ±2 | 16 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DXB# |
| AD5543BRMZ-REEL7 | ±2 | 16 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DXB# |
| AD5553CRM | ±1 | 14 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DUC |
| AD5553CRM-REEL7 | ±1 | 14 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DUC |
| AD5553CRMZ[2] | ±1 | 14 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DUC# |
| AD5553CRMZ-REEL7[2] | ±1 | 14 | −40°C to +85°C | 8-Lead MSOP | RM-8 | DUC# |

[1] The AD5543 contains 1040 transistors. The die size measures 55 mil × 73 mil or 4,015 sq. mil.
[2] Z = RoHS Compliant Part, # denotes RoHS Compliant product may be top or bottom marked.

## NOTES